Clean Version of Pending Claims

CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR
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Claims 20-56, as of March 21, 2000 (*date response to first office action filed).*

20. (Once Amended) A method of fabricating a memory array, the method comprising the steps of:

forming a number of access transistors, each access transistor formed in a pillar of semiconductor material that extends outwardly from a substrate wherein each access transistor includes, in order, a first source/drain region, a unitary body region and a second source/drain region formed vertically thereupon;

forming a trench capacitor, wherein a first plate of the trench capacitor is integral with the first source/drain region of the access transistor;

forming a number of word lines in a number of trenches that separate adjacent rows of access transistors, wherein each trench includes two word lines with a gate of each word line interconnecting alternate access transistors on opposite sides of the trench;

forming a number of bit lines that interconnect second source/drain regions of selected access transistors.

21. The method of claim 20, wherein the step of forming a trench capacitor further includes the step of forming a second plate that surrounds the first plate.

22. The method of claim 20, and further comprising the step of forming a contact that couples a second plate of the trench capacitor to an underlying semiconductor layer.

23. The method of claim 20, where the step of forming a trench capacitor comprises the step of forming a second plate that forms a grid pattern in a layer of semiconductor material such that the grid surrounds each of the pillars that form the access transistors.

24. The method of claim 20, wherein the step of forming a trench capacitor comprises the step of depositing poly-silicon in crossing row and column isolation trenches formed around the pillars that define the access transistors.

25. A method of fabricating a memory array, the method comprising the steps of:

forming a first conductivity type first source/drain region layer on a substrate;

forming a second conductivity type body region layer on the first source/drain region layer;

forming a first conductivity type second source/drain region layer on the body region layer;

forming a plurality of substantially parallel column isolation trenches extending through the second source/drain region layer, the body region layer, and the first source/drain region layer, thereby forming column bars between the column isolation trenches;

forming a plurality of substantially parallel row isolation trenches, orthogonal to the column isolation trenches, extending to substantially the same depth as the column isolation trenches, thereby forming an array of vertical access transistors for the memory array;

filling the row and column isolation trenches with a conductive material to a level that does not exceed the lower level of the body region so as to provide a common plate for capacitors of memory cells of the memory array;

forming two conductive word lines in each row isolation trenches that selectively interconnect alternate access transistors on opposite sides of the row isolation trench; and

forming bit lines that selectively interconnect the second source/drain regions of the access transistors on each column.

26. The method of claim 25, wherein the step of forming the first conductivity type source/drain region layer on the substrate comprises the step of forming the first conductivity type first source/drain region layer outwardly from the substrate to a distance sufficient for the first source/drain region layer to also function as a first plate of the capacitor for each memory cell in the array.

27. The method of claim 20, wherein the memory array comprises memory cells each occupying an area of $4F^2$, wherein F is a minimum feature size.

28. The method of claim 20, wherein the first source/drain region is N+ doped.

29. The method of claim 28, including forming the first source/drain region to a thickness of approximately 3.5 micrometers.

30. The method of claim 28, wherein the unitary body region is P- doped.

31. The method of claim 30, including forming the unitary body region by epitaxial growth of single-crystalline P- silicon to a thickness of approximately 0.5 microns.

32. The method of claim 30, wherein the second source/drain region is N+ doped.

33. The method of claim 32, including forming the second source/drain region by implanting the N+ dopant to a depth of approximately 0.1 microns.

34. The method of claim 25, wherein the memory array comprises memory cells each occupying an area of $4F^2$, wherein F is a minimum feature size.

35. The method of claim 25, wherein the first source/drain region is N+ doped.

36. The method of claim 35, including forming the first source/drain region to a thickness of approximately 3.5 micrometers.

37. The method of claim 35, wherein the unitary body region is P- doped.

38. The method of claim 37, including forming the unitary body region by epitaxial growth of single-crystalline P- silicon to a thickness of approximately 0.5 microns.

39. The method of claim 37, wherein the second source/drain region is N+ doped.

40. The method of claim 39, including forming the second source/drain region by implanting the N+ dopant to a depth of approximately 0.1 microns.

41. A method of forming an array of memory cells upon a substrate, the method comprising:

forming a plurality of isolated vertical access transistors separated by trenches, comprising in order outward from the substrate, a first source drain region, a unitary body region, and a second source/drain region, wherein the separation of trenches is such that the area occupied by each memory cell is $4F^2$, wherein F is a minimum feature size;

forming a trench capacitor for each memory cell, wherein a portion of the first source/drain region serves as a first plate of the capacitor;

forming two word lines in select trenches, with a gate of each word line interconnecting alternate access transistors on opposite sides of the trench; and

forming bit lines that interconnect select second source/drain regions.

42. The method of claim 41, wherein the first source/drain region is N+ doped.

43. The method of claim 41 including forming the first source/drain region to a thickness of approximately 3.5 micrometers.

44. The method of claim 42, wherein the unitary body region is P- doped.

45. The method of claim 43, including forming the unitary body region by epitaxial growth of single-crystalline P- silicon to a thickness of approximately 0.5 microns.

46. The method of claim 44, wherein the second source/drain region is N+ doped.

47. The method of claim 46, including forming the second source/drain region by implanting the N+ dopant to a depth of approximately 0.1 microns.

48. The method of claim 41, wherein forming the trench capacitor further includes the step for forming a second plate that surrounds the first plate.

49. A method of forming an array of memory cells on a substrate, the method comprising:

forming atop the substrate a first layer of a first conductivity type of single crystalline silicon, a second layer of a second conductivity type of single crystalline silicon, and a third layer of the first type of single crystalline silicon;

selectively etching through the third through first layers and partially into the substrate so as to form a plurality of trenches and pillars spaced apart such that the surface area occupied by each memory cell is $4F^2$, wherein F is a minimum feature size;

filling the trenches with a conductive material so as to provide for a common plate for capacitors associated with each memory cell, such that a portion of the first layer in each pillar serves as a plate for the capacitor;

electrically interconnecting select pillars by word lines electrically coupled to the second

layer of the select pillars;

electrically interconnecting the select pillars by bit lines electrically coupled to the third layer of the select pillars.

50. A method according to claim 46, wherein the first conductivity type is N+ and the second conductivity type is P-.

51. A method of fabricating an array of memory cells on substrate, the method comprising:

forming spaced apart access transistors isolated by trenches, each access transistor comprising in order from the substrate outward, an N+ - doped first source/drain region, a P- doped body region and an N+ -doped second source/drain region;

forming capacitors in the trench corresponding to each access transistor, wherein a portion of the N+ -doped first source/drain region adjacent the substrate serves as a plate for the capacitor corresponding to each access transistor; and

electrically connecting the access transistors in a manner that allows for an electrical charge to be accessed or stored in each capacitor via the corresponding transistor.

52. A method according to claim 51, wherein electrically connecting the access transistors includes:

forming a number of word lines in a number of trenches , wherein each trench includes two word lines with a gate of each word line interconnecting alternate access transistors on opposite sides of the trench; and

forming a number of bit lines that interconnect second source/drain regions of selected access transistors.

53. A method of forming a memory device having an array of memory cells and a minimum feature size F, comprising:

forming a plurality of vertical access transistors separated by trenches and laid out in a substantially checker-board pattern such that the memory cells occupy an area of $4F^2$, wherein the formation of the vertical access transistors consists of the steps forming a first source/drain region of a first dopant type, forming a body region of a second dopant type atop the first source/drain region, and forming a second source/drain region of a second dopant type atop the body region;

forming a capacitor in the trenches by lining the trench with a gate oxide and then filling the trench with polysilicon of the first type so as to surround a portion of the first source/drain region such that the surrounded portion of the first source/drain region serves as a first plate of the capacitor and the polysilicon in the trench serves as a second plate of the capacitor; and

electrically connecting the transistors via bit lines and word lines so as to provide the capability of accessing a charge stored in one or more of the capacitors or providing a charge thereto.

54. The method of claim 53, further including connecting the word lines to a word line decoder and the bit lines to a bit line decoder to provide selective access to the memory cells.

55. A method of forming an electronic device having an array of memory cells and a minimum feature size F, comprising:

forming on a substrate a plurality of spaced apart access transistors each comprising in order outward from the substrate, a first layer of N+ dopant serving as first source/drain, a second layer of P- dopant serving as a body region and a third layer of N+ dopant serving as a second source/drain region;

wherein the forming of the access transistors includes the step of forming trenches therebetween so as to provide a memory cell area of $4F^2$;

forming, for each transistor, a capacitor in the trenches by filling the trench with a thin layer of oxide and polysilicon such that a portion of the first source/drain, the oxide layer and the

polysilicon respectively serve as a first plate, a dielectric, and a second plate for the capacitor

electrically connecting the transistors with word lines and bit lines;

connecting the word lines to a word line decoder;

connecting the bit lines to a bit line decoder;

operatively connecting the word line and bit line decoders to an address buffer; and

interfacing the address buffer to an electronic system via address lines.

56. The method of claim 55, wherein the electronic system is a microprocessor.

input/output circuitry that is coupled to bit lines BL-1 through BL-M and complement bit lines BL-1* through BL-M*of array 110. Address buffer 114 also is coupled to control word line decoder 116. Word line decoder 116 and bit line decoder 118 selectably access memory cells 112-*ij* in response to address signals that are provided on address lines 120 from electronic system 101 during write and read operations.

In operation, memory 100 receives an address of a particular memory cell at address buffer 114. For example, electronic system 101 may provide address buffer 114 with the address for cell 112-11 of array 110. Address buffer 114 identifies word line WL-1 for memory cell 112-11 to word line decoder 116. Word line decoder 116 selectively activates word line WL-1 to activate access transistor 130-1*j* of each memory cell 112-1*j* that is connected to word line WL-1. Bit line decoder 118 selects bit line BL-1 for memory cell 112-11. For a write operation, data received by input/output circuitry is coupled to bit lines BL-1 through access transistor 130-11 to charge or discharge storage capacitor 132-11 of memory cell 112-11 to represent binary data. For a read operation, bit line BL-1 of array 110 is equilibrated with bit line BL-1*. Data stored in memory cell 112-11, as represented by the charge on its storage capacitor 132-11, is coupled to bit line BL-1 of array 110. The difference in charge in bit line BL-1 and bit line BL-1* is amplified, and a corresponding voltage level is provided to the input/output circuits.

Figures 2 through 4 illustrate an embodiment of a memory cell with a vertical transistor and trench capacitor for use, for example, in memory device 100 of Figure 1. Specifically, Figure 2 is a plan view of a layout of a number of memory cells indicated generally at 202A through 202D in array 200. Figure 2 depicts only four memory cells. It is understood, however, that array 200 may include a larger number of memory cells even though only four are depicted here.

Each memory cell is constructed in a similar manner. Thus, only memory cell 202C is described herein in detail. Memory cell 202C includes pillar 204 of single crystal semiconductor material, e.g., silicon, that is divided into second source/drain region 206, body region 208, and first source/drain region 210 to form access transistor 211.

Pillar 204 extends vertically outward from substrate 212 of, for example, p- silicon. Second source/drain region 206 and first source/drain region 210 each comprise, for example, n + silicon and body region 208 comprises p- silicon.

Word line 212 passes body region 208 of access transistor 211 in isolation trench 214. Word line 212 is separated from body region 208 of access transistor 211 by gate oxide 216 such that the portion of word line 212 adjacent to body region 208 operates as a gate for access transistor 211. Word line 212 may comprise, for example, n+ poly-silicon material that is deposited in isolation trench 214 using an edge-defined technique such that word line 212 is less than a minimum feature size, F, for the lithographic technique used to fabricate array 200. Passing word line 213 is also formed in trench 214. Cell 202C is coupled with cell 202B by bit line 218.

Memory cell 202C also includes storage capacitor 219 for storing data in the cell. A first plate of capacitor 219 for memory cell 202C is integral with first source/drain region 210 of access transistor 211. Thus, memory cell 202C may be more easily realizable when compared to conventional vertical transistors since there is no need for a contact between first source/drain region 210 and capacitor 219. Second plate 220 of capacitor 219 is common to all of the capacitors of array 200. Second plate 220 comprises a mesh or grid of n+ poly-silicon formed in deep trenches that surrounds at least a portion of first source/drain region 210 of each pillar 204A through 204D. Second plate 220 is grounded by contact with substrate 212 underneath the trenches. Second plate 220 is separated first source/drain region 210 by gate oxide 222.

With this construction for memory cell 202C, access transistor 211 is like a silicon on insulator device. Three sides of the transistor are insulated by thick oxide in the shallow trench. If the doping in pillar 204 is low and the width of the post is sub-micron, then body region 208 can act as a "fully-depleted" silicon on insulator transistor with no body or substrate to contact. This is desirable to avoid floating body effects in silicon on insulated transistors and is achievable due to the use of sub-micron dimensions in access transistor 211.

Figure 4 is a schematic diagram that illustrates an effective circuit diagram for the embodiment of Figures 2 and 3. It is noted that storage capacitor 219 formed by first source/drain region 210 and second plate 220 is depicted as four separate capacitors. This represents that the first plate 220 surrounds second source/drain region 210 which increases the charge storage capacitance and stored charge for the memory cell. It is also noted that second plate 220 is maintained at a constant potential, e.g., ground potential.

As shown in Figure 2, the memory cells of array 200 are four-square feature ($4F^2$) memory cells. Using cell 202D as an example, the surface area of cell 202D is calculated based on linear dimensions in the bit line and word line directions. In the bit line direction, the distance from one edge of cell 202D to a common edge of adjacent cell 202A is approximately 2 minimum feature sizes (2F). In the word line direction, the dimension is taken from the midpoint of isolation trenches on either side of memory cell 202D. Again, this is approximately two minimum feature sizes (2F). Thus, the size of the cell is $4F^2$. This size is much smaller than the current cells with stacked capacitors or trenched capacitors.

Figures 5A through 5M illustrate one embodiment of a process for fabricating an array of memory cells, indicated generally at 299, according to the teachings of the present invention. In this example, dimensions are given that are appropriate to a 0.2 micrometer lithographic image size. For other image sizes, the vertical dimensions can be scaled accordingly.

As shown in Figure 5A, the method begins with substrate 300. Substrate 300 comprises, for example, a P-type silicon wafer, layer of P- silicon material, or other appropriate substrate material. Layer 302 is formed, for example, by epitaxial growth outwardly from layer 300. Layer 302 comprises single crystalline N+ silicon that is approximately 3.5 micrometers thick. Layer 304 is formed outwardly from layer 302 by epitaxial growth of single crystalline P- silicon of approximately 0.5 microns. Layer 306 is formed by ion implantation of donor dopant into layer 304 such that layer 306 comprises single crystalline N+ silicon with a depth of approximately 0.1 microns.